REMARKS

Drawing Rejection under U.S.C. § 1.83(a)

The drawings were objected to under 37 U.S.C. § 1.83(a), as not showing the features of claims 16-17, 20, 23 and 25-26. Applicant traverses this rejection. It is not known to which features the Examiner is referring. Regarding claims 16, 25 and 26, the memory array and control circuitry are clearly shown for example in Figures 1A and 32. The block array architecture of claim 17 is shown in Figures 1A, 15 and 32. The load command register cycle, active cycle and write cycles of claims 20 and 23 are illustrated for example in Figure 30.

Applicant requests that the objection be withdrawn.

Rejection Under U.S.C. § 112, first paragraph

Claims 1-27 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses this rejection.

The Examiner states that claims 1-27 are not understood because some elements of Figures 1A, 1B and 1C are not specifically described in the specification. Applicant has enclosed a red-line copy of Figure 1A removing protect circuit 149, low Vcc circuit 125 and latch 127. These circuits are superfluous and are removed to improve the focus of the Figure.

The Examiner states some of the features of the Figures are not fully described in the specification. Applicant believes that relevant features of the Figures have been described in the specification to allow one skilled in the art to practice the invention. Each of the Figures are described in the specification in different levels of specificity, however, Applicant does not believe that relevant features have been illustrated but not described.

Regarding Figure 32, the connective relationship of control circuit 340 has been described in the specification, page 41, line 7 to page 43, line 7. Clearly one skilled in the art recognizes

that electrical connections exist between the control circuit of the block diagram and other circuits of the memory. Applicant does not believe the connections are needed to understand the invention or claims, but has amended Figure 32 in the attached red-line version to show some general connectivity.

Applicant requests that the rejection of the claims 1-27 be withdrawn because the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Rejection Under U.S.C. § 112, second paragraph

Claims 5 and 8 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses.

Claim 5 recites "latching the write data in a write latch on the first clock cycle" which does properly refer to the " the first clock cycle" of claim 4.

Claim 8 has been amended to correct antecedent basis.

Rejection Under U.S.C. §103

Claims 1-27 were rejected under 35 U.S.C. § 103 as being unpatentable over Patel, U.S. Patent No. 5,539,696.

Applicant respectfully traverses this rejection. Specifically, Patel teaches a synchronous memory device that allows faster burst data write operations by using parallel latches of the input buffers, see column 5, line 64 to column 6, line 26. The banks of the memory array are divided into column independent sections that are simultaneously written to from the buffer parallel latches.

The Examiner notes that the references indicates that data can be written to or read from the memory, citing column 5, lines 1-44, and other sections. The Examiner then states that the memory system obviously can be capable of performing a data write operation on bank A on a first clock cycle and performing a read operation on bank B on the next clock cycle.

Applicant traverses the rejection. Specifically, the presence of synchronous dynamic memory devices that can be written or read in a burst mode does not make the present invention

obvious. There is no discussion in Patel of the timing between write and read operations. That is, absent a specific teaching to change the basic operation of a synchronous dynamic memory device, one skilled in the art is not motivated to change prior systems. It is well known in the synchronous dynamic memory art that there is a minimum time (such as write recovery and precharge times) that prohibit read operations from immediately following a write operation.

The Examiner states that the desired programming of a memory control circuit 28 of Patel can change operation specifications. This fails to recognize operational limitations of the memory device of Patel. The present invention is a non-volatile memory not a volatile memory as Patel. As such, pre-charge times are not needed between write and read operations. Internal write latches (see Figure 32) are provided to latch input data and free the external data connections. Further, the memory device has bank independent read and write capabilities. These features eliminate prior write recovery times and allows the read to immediately follow a write command and corresponding data. Applicant refers to Figures 30 and 9 for illustrations of the read and write timing of the present invention.

Applicant maintains that the cited reference does not teach or suggest the present claims. Further, there is no motivation taught to modify known synchronous memory operation. Applicant respectfully requests the allowance of the present claims.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that all claims are in condition for allowance and requests reconsideration of the application and allowance of claims.

The Examiner is invited to contact Applicant's attorney to discuss any questions that may remain with respect to the present application.

Respectfully submitted,

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MARKED-UP COPY OF CLAIMS

IN THE SPECIFICATION

On page 42, line 5, after "control circuit" please insert --340-- as follows:

A data buffer 330 can be coupled to the data communication connections to manage the bi-directional data communication. This buffer can be a traditional FIFO or pipelined input/output buffer circuit. The write latch is coupled between the data buffer and the memory array to latch data provided on the data communication connections. Finally, a control circuit 340 is provided to manage the read and write operations performed on the array.

IN THE CLAIMS

8. (Amended) The method of claim 6 further comprises:

receiving a row address on a first clock cycle;

receiving a column address on a second clock [signal] cycle following the first clock [signal] cycle, wherein the write data is received on the data connections on the second clock cycle.